METHODS AND STRUCTURES FOR PROVIDING PROGRAMMABLE WIDTH AND ERROR CORRECTION IN MEMORY ARRAYS IN PROGRAMMABLE LOGIC DEVICES

ABSTRACT

A random access memory (RAM) in a programmable logic device (PLD) supports error correction as well as a configurable data width. The number of bits in a user data word varies by the selected configuration of the RAM, while the number of bits in the error correction code (ECC) is unvarying, and is based on the total width of the memory. In some embodiments, separate ports are provided for the user data and the ECC data. Thus, ECC data can be written to an ECC portion of the RAM array at a given RAM address, while at the same time user data is written to or read from a configurable user data portion of the RAM array at the same RAM address. In other embodiments, a single memory access port is used for both user data and ECC data.